General Description

The HE24C02N is 2-Kbit I^2C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 256 × 8bits, which is organized in 8 bytes per page. HE24C02N provides the following devices for different application.

Features

- Single Supply Voltage and High Speed
  - Minimum operating voltage down to 1.6V
  - 1 MHz clock from 2.5V to 5.5V
  - 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  - Read current 400uA, maximum
  - Write current 1.6mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Package: SOP8, TSSOP8, SOT23-5
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: > 1 Million Write Cycles
  - Data Retention: > 100 Years
  - ESD HBM: 4KV
  - Latch-up Capability: +/- 200mA

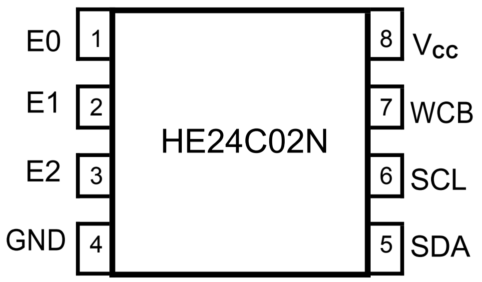
Device Selection Table

Device Name	Voltage Range	Temp. Range	Max. Clock Frequency
HE24C02N -LI	1.6V~5.5V	-40°C ~ 85°C	1MHz[1]
HE24C02N -MI	1.7V~5.5V	-40°C ~ 85°C	1MHz[1]

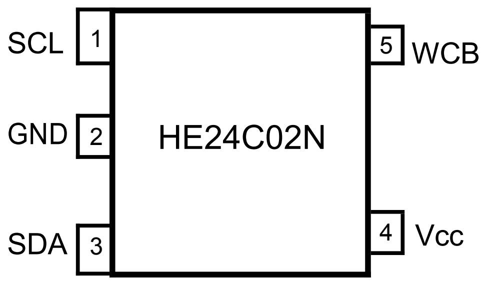
Note 1: 400 kHz for VCC < 2.5V.

Pin Configuration

Figure 1-1 Pin Configuration



SOP8/ TSSOP8



SOT23-5

Pin Definition

Table 1-1 Pin Definition

Pin	Name	Type	Description
1	E0	I/O	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	GND	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	V_{CC}	Power	Power

P Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

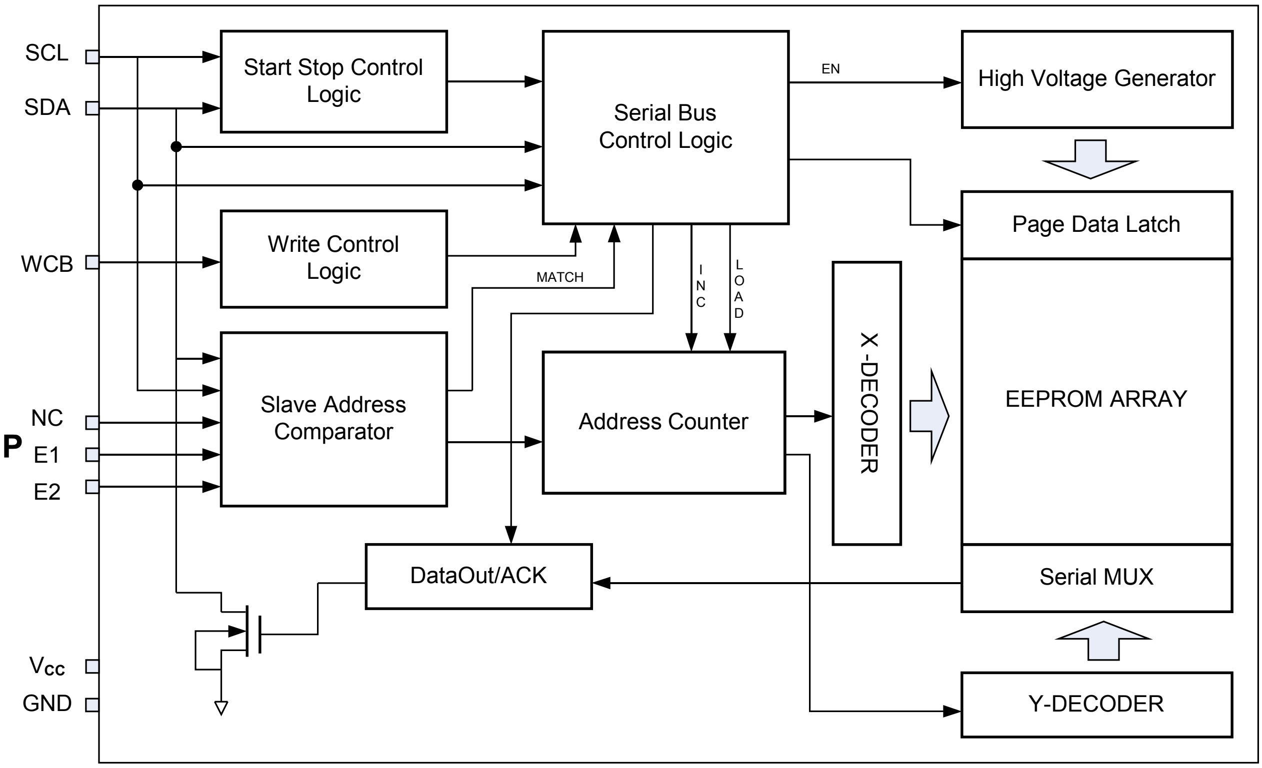
Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (E2, E1, E0): The E2, E1 and E0 pins are device address inputs. Typically, the E2, E1 and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1 and E0 pins will be internally pulled down to GND.

Write Control (WCB): The Write Control input, when WCB is connected directly to V_{CC}, all write operations to the memory are inhibited. When connected to GND, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to GND.

Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Absolute Maximum Ratings

- Storage Temperature..........................-65°C to +150°C
- Operation Temperature........................-40°C to +85°C
- Maximum Operation Voltage.......................V
- Voltage on Any Pin with
  Respect to Ground.....................................V to (Vcc+1.0) V
- DC Output Current...............................5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-1 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (E0, E1,E2,WCB,SCL)	6	pF	V_{IN}=GND

Note: [1] Test Conditions: T_A = 25°C, F = 1MHz, Vcc = 5.0V.

Table 3-2 DC Characteristics （Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 85°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
		1.6	-	5.5	V	HE24C02N-LI
		1.7	-	5.5	V	HE24C02N-MI
Isb	Standby Current	-	-	1.0	uA	Vcc = 3.3V, T_A = 85°C
		-	-	3.0	uA	Vcc = 5.5V, T_A = 85°C
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc=5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	0.8	1.6	mA	Vcc=5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = V_{CC} or GND
V_{IL}	Input Low Level	–0.6	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-3 AC Characteristics

（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 85°C, C_L=100pF, Test Conditions are listed in Notes [2]）

Symbol	Parameter	1.7≤V_{CC}<2.5			2.5≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- ✧ R_L (connects to V_{CC}): 1.3k (2.5V, 5.5V), 10k (1.7V)
- ✧ Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- ✧ Input rise and fall times: ≤50ns
- ✧ Input and output timing reference voltages: 0.5V_{CC}

Table 3-4 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

Figure 3-1 Bus Timing

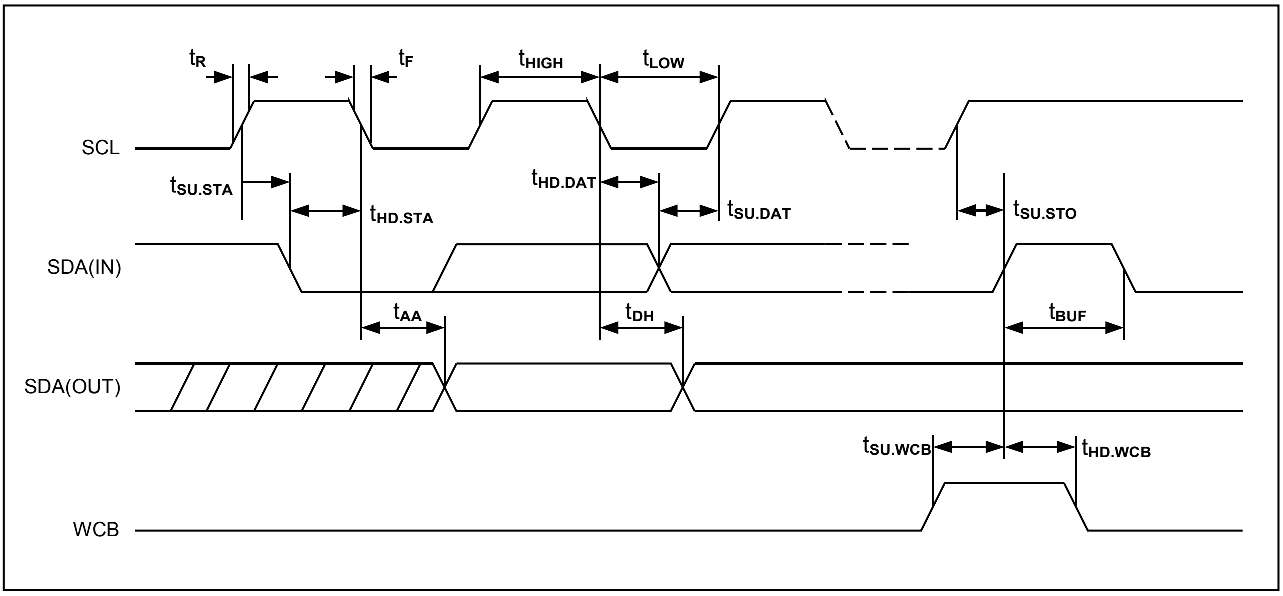
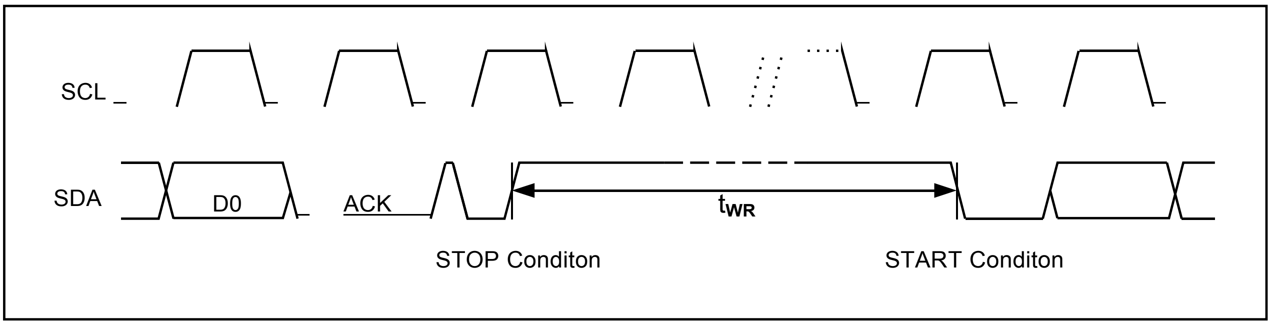


Figure 3-2 Write Cycle Timing



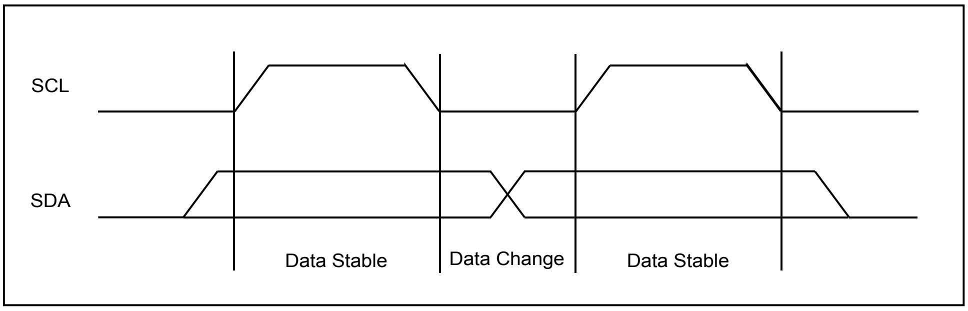
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 4-1 Data Validity



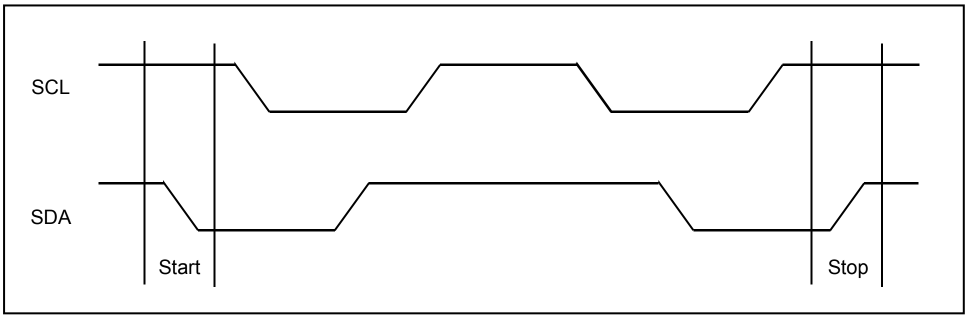
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the HE24C02N in a standby power mode (see Figure 4-2).

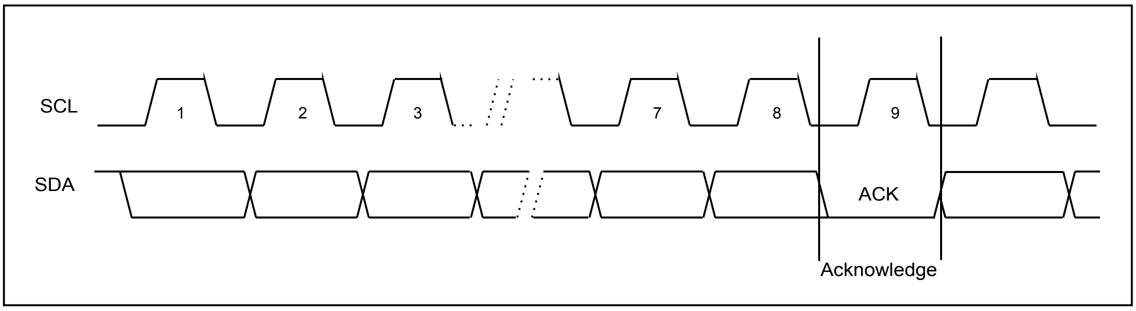
Figure 4-2 Start and Stop Definition



4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the HE24C02N in 8-bit words. The HE24C02N sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 4-3 Output Acknowledge



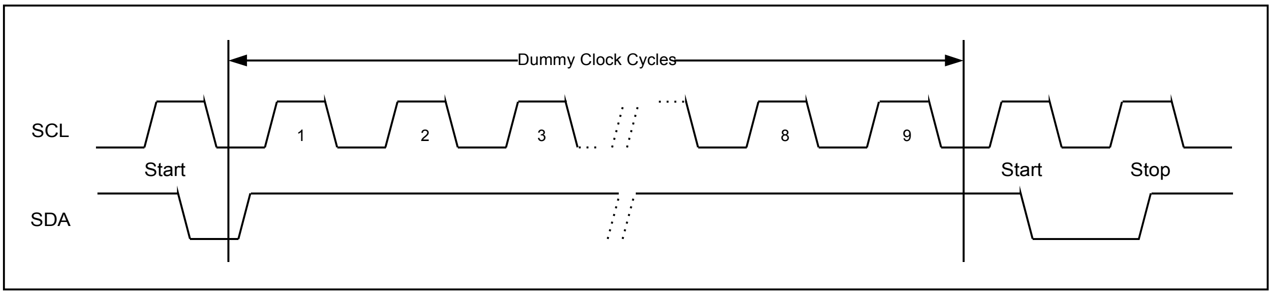
4.5 Standby Mode

The HE24C02N features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Addressing

The HE24C02N requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	E2	E1	E0	R/W

Table 4-2 Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	A7	A6	A5	A4	A3	A2	A1	A0

The E2, E1 and E0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.
The E2, E1 and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.8 Data Security

HE24C02N has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

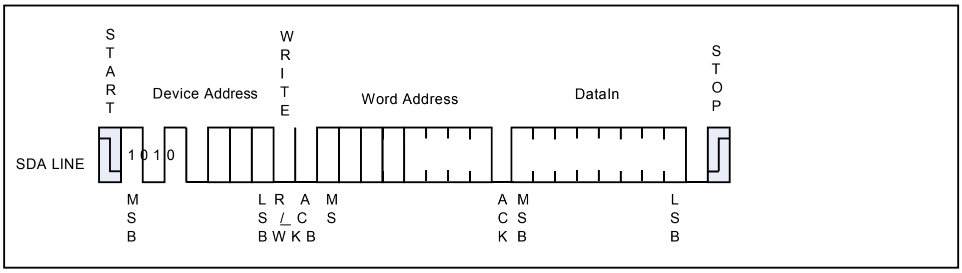
5. Instructions

5.1 Write Operations

5.1.1 BYTE WRITE

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the HE24C02N will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the HE24C02N will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the HE24C02N enters an internally timed write cycle, all inputs are disabled during this write cycle and the HE24C02N will not respond until the write is complete (see Figure 5-1).

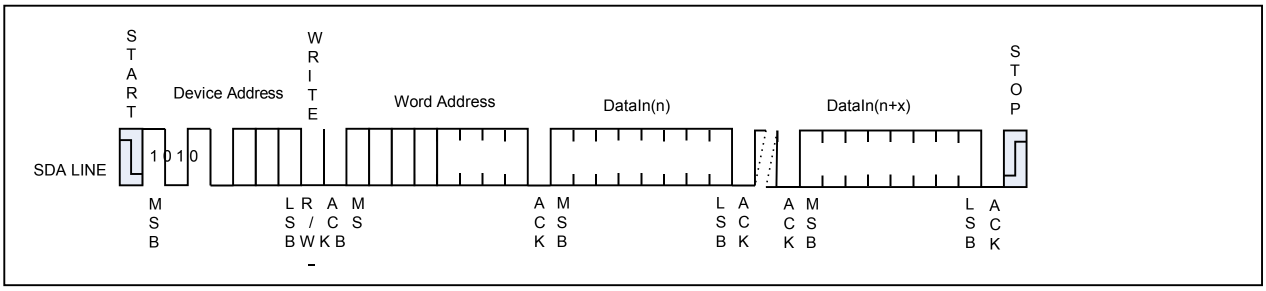
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the HE24C02N acknowledges receipt of the first data word, the master can transmit more data words. The HE24C02N will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower three bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the HE24C02N, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the HE24C02N inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the HE24C02N respond with a "0", allowing the read or write sequence to continue.

5.2 Read Operations

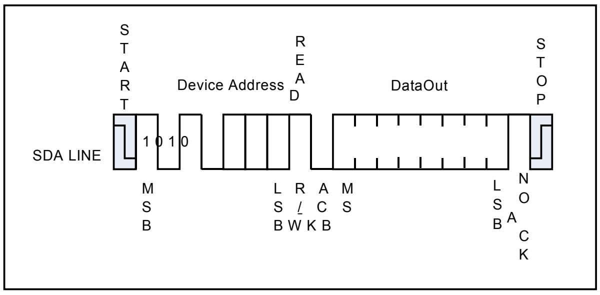
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the HE24C02N, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 5-3).

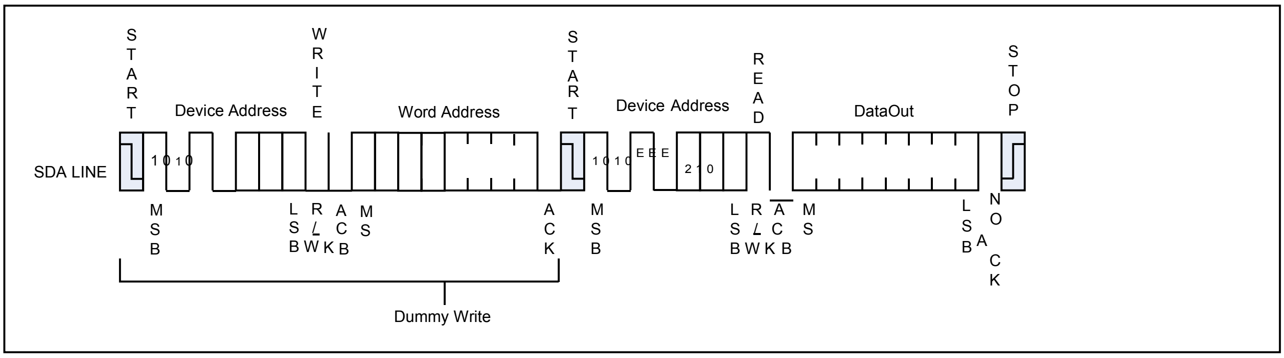
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the HE24C02N, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The HE24C02N acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-4).

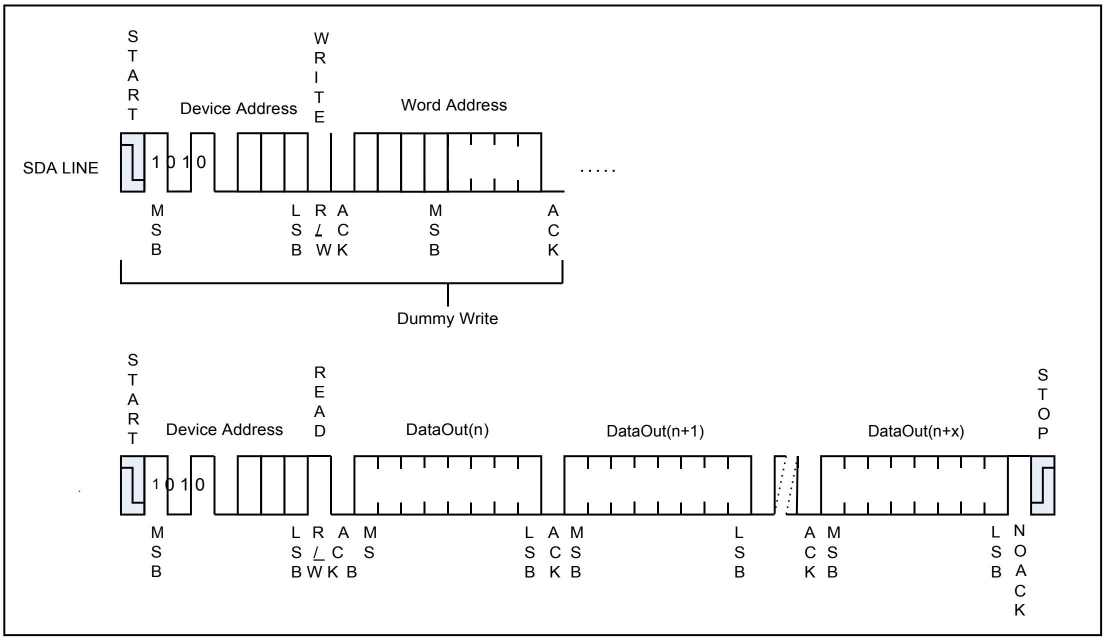
Figure 5-4 Random Read



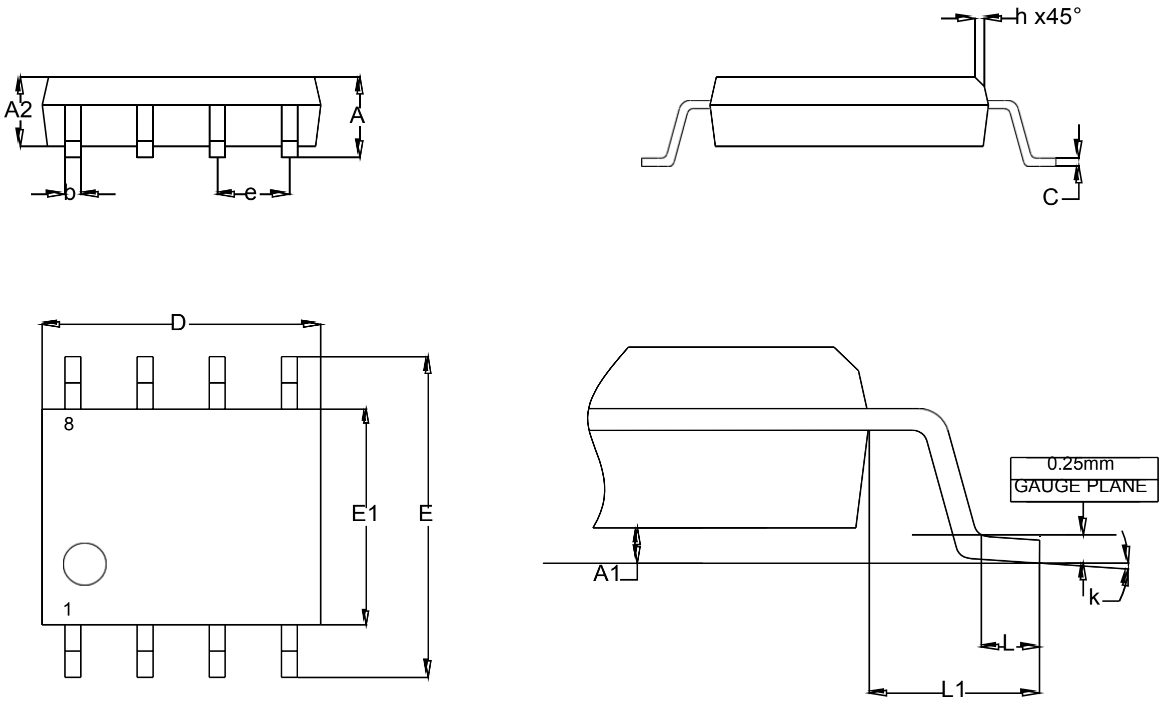
5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the HE24C02N receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-5)

Figure 5-5 Sequential Read



7.2 8-lead SOP



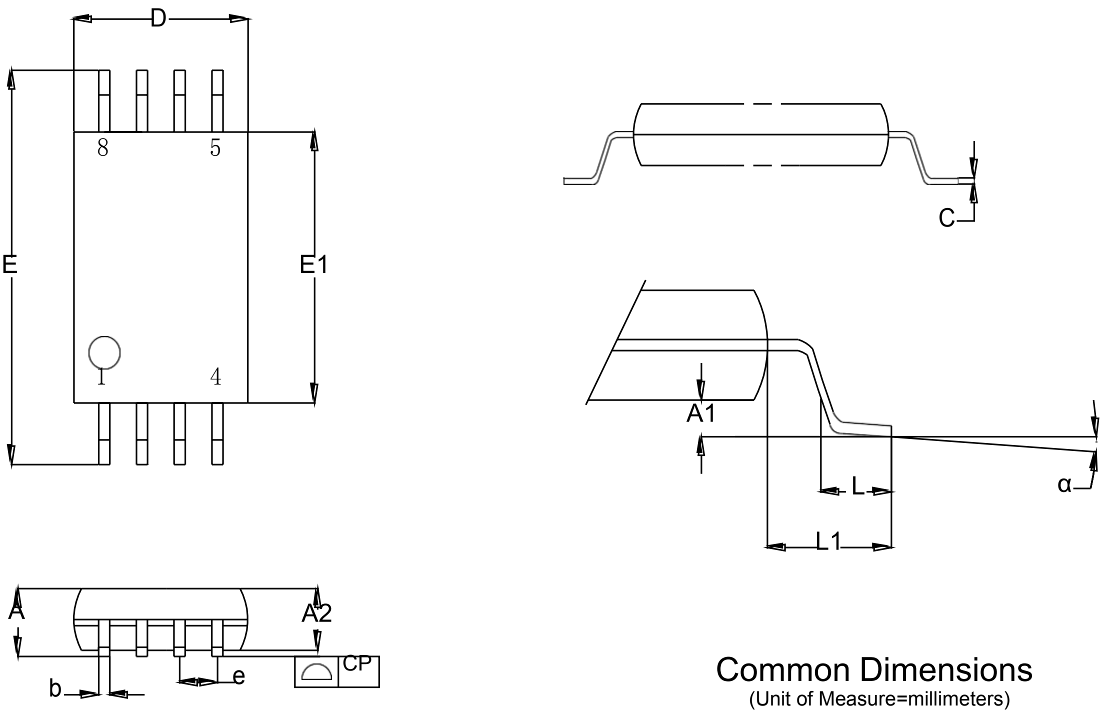
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.280	-	0.480
c	0.170	-	0.230
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
h	0.250	-	0.500
k	0°	-	8°
L	0.400	-	1.270
L1	-	1.040	-

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
	8-lead SOP	SP-8	A

7.3 8-lead TSSOP



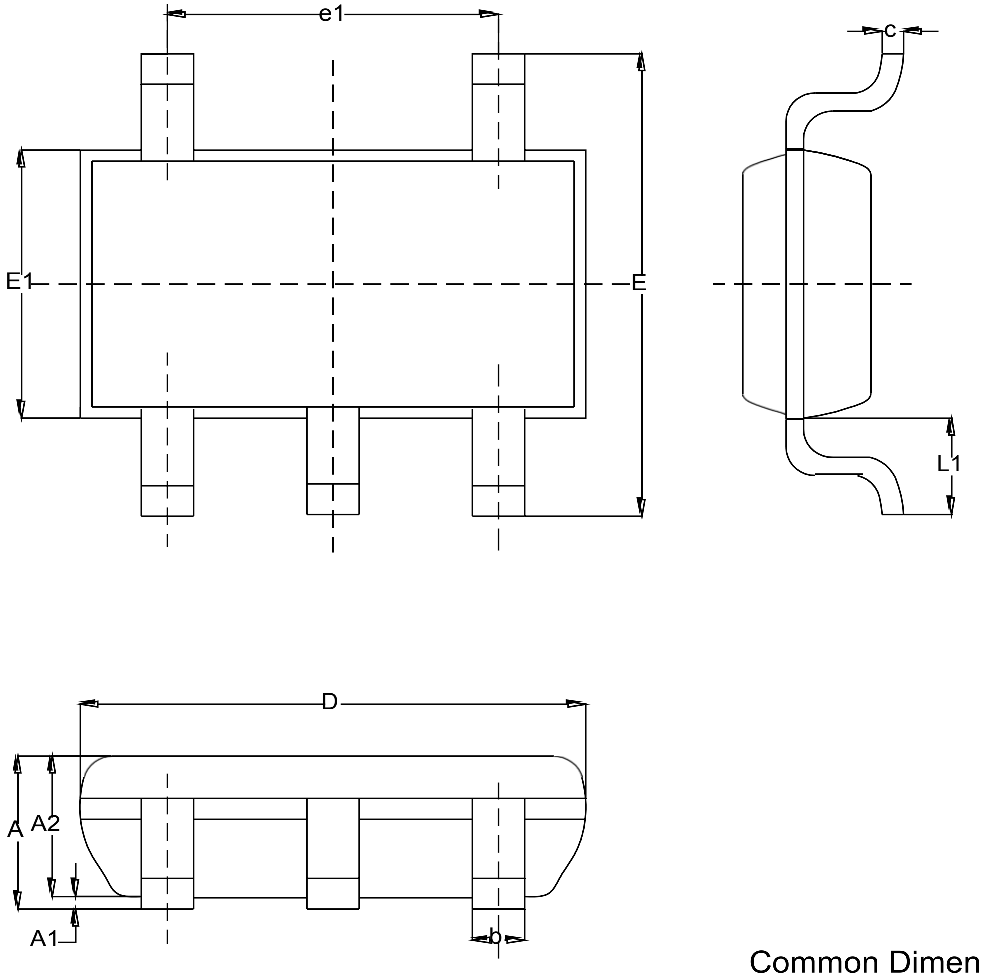
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
CP	-	-	0.100
D	2.900	3.000	3.100
e	-	0.650	-
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
L	0.450	0.600	0.750
L1	-	1.000	
α	0°	-	8°

Note：1. Dimensions are not to scale

	TITLE 8-lead TSSOP	DRAWING NO. TS-8	REV A

7.4 SOT23-5



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.000	-	1.250
A1	0.030	-	0.090
A2	1.050	-	1.150
c	0.080	-	0.200
D	0.290BSC		
E	2.800BSC		
E1	1.600BSC		
e	0.950BSC		
e1	1.900BSC		
L1	0.600REF		
b	0.300	-	0.450

Note： 1. Dimensions are not to scale

	TITLE SOT23-5L	DRAWING NO. ST-5	REV A